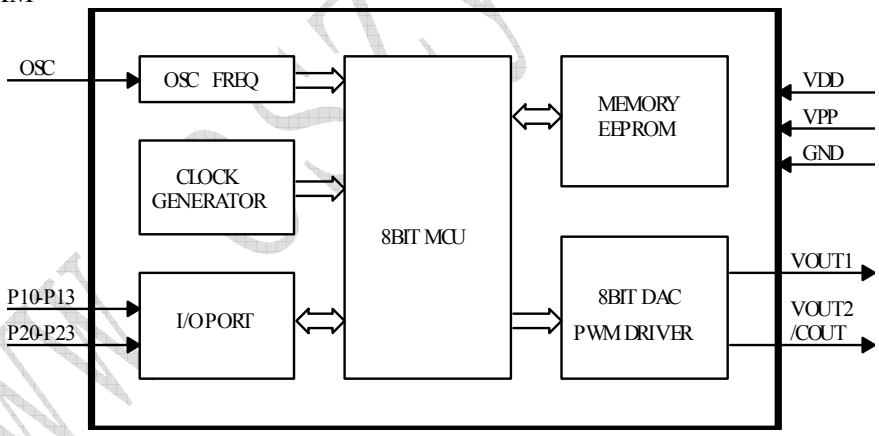
FEATURES

Standard CMOS process.
Embedded EPROM.
Embedded 8-bit MCU.
10, 20, 40 and 80sec voice duration at 6 KHz sampling with 4-bit ADPCM compression.
Combination of voice building blocks to extend playback duration.
Table entries are available for voice block combinations.
User selectable PCM or ADPCM data compress.
Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
Programmable I/Os, Timer Interrupt and Watch Dog Timer.
Built-in oscillator to control sampling frequency with an external resistor.
2.2V – 3.6V single power supply and < 5uA low stand-by current.
PWM Vout1 and Vout2 drive speaker directly.
D/A COUT with ramp-up ramp-down option to drive speaker through an external BJT.

DESCRIPTION

ABT' A91XX is a 8-bit CPU based Voice chip series. It is fabricated with Standard CMOS process with embedded voice storage memory. It can store from 10 to 80 sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 8-bit PCM is also available as user selectable option to improve sound quality. Depending on IC body, there are up to twelve programmable I/O pins. Key trigger and Parallel CPU trigger mode can be configured according to different application requirement. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 8-bit current mode D/A output and PWM direct speaker driving output minimize the number of external components.

BLOCK DIAGRAM



IC BODY PACKAGE&I/O LIST

Part No.	Second(s)	DIP8	SOP8	DIP16	SOP16	Coding DICE	COB
A9110	10"	2 I/O	2 I/O	4 I/O		√	√
A9121	20"	2 I/O	2 I/O	4 I/O		√	√
A9142	**40"**	**2 I/O**	**2 I/O**	**8I/O**	**--**	**√**	**√**
A9185	80"	2 I/O	2 I/O	8I/O	--	√	√

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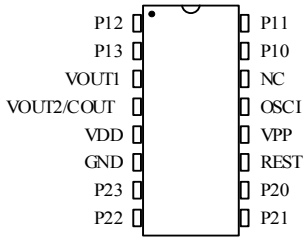
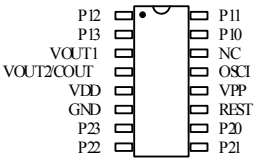
PIN CONFIGURATIONS

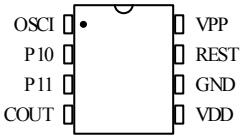
DIP16 300mil



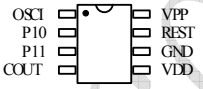
SOP16 300mil



DIP8 300mil



SOP8 150mil



PIN DESCRIPTIONS

Pin Names	Description
VOUT1	PWM output to drive speaker directly
VOUT2/COUT	PWM output or COUT DAC output select by programmable option
GND	Power Ground
OSC	Oscillator input
VPP	Program Power Supply
VDD	Positive Power Supply
P10-13	Programmable I/O pins
P20-23	Programmable I/O pins
REST	Reset pin, Low active

Note:
P10-13 and P20-23 are software programmable I/O pins that can be set to different configurations such as pure input, input with pull-up, input with pull-down and output. But the programmable I/O pins set up will not take effect after RESET. It will take effect only when the chip operated at least once time after RESET. Pin Status after Reset:
P10-13 and P20-23 Input and Floating (will draw stand-by current if leave open).
VOUT1, VOUT2 – Tristate output with 100K pull-low.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
VDD - GND	-0.5 ~ +3.8	V
VIN	VSS -0.3<VIN<VDD + 0.3	V
VOUT	VSS <VOUT<VDD	V
T (Operating):	-40 ~ +85	℃
T (Junction)	-40 ~ +125	℃
T (Storage)	-55 ~ +125	℃

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DC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.0V, V_{SS} = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	2.2	3.0	3.6	V	
ISB	Standby current	｝	1	5	μA	I/O properly terminated
IOP	Operating current	｝	｝	15	mA	I/O properly terminated
VIH	"H" Input Voltage	2.5	3.0	3.5	V	VDD=3.0V
VIL	"L" Input Voltage	-0.3	0	0.5	V	VDD=3.0V
IVOUTL	VOUT low O/P Current	｝	130	｝	mA	Vout=1.0V
IVOUTH	VOUT high O/P Current	｝	-130	｝	mA	Vout=2.0V
ICO	COUT O/P Current	｝	-2	｝	mA	Data = 80h
IOH	O/P High Current	｝	-8	｝	mA	VOH=2.5V
IOL	O/P Low Current	｝	8	｝	mA	VOL=0.3V
RNVOUT	VOUT pull-down resistance	｝	100K	｝	Ω	VOUT pin set to internal pull-down
RNPIO	Programmable IO pin pull-down resistance	｝	1M	｝	Ω	PBx, PCx, PDx set to internal pull-down
RUPIO	Programmable IO pin	3.3K	4.7K	｝	Ω	PBx, PCx, PDx set to
	pull-up resistance					internal pull-up
ΔFc/Fc	Chip to chip Frequency Variation	-5	｝	+5	%	Also apply to lot to lot variation

Note:

1. C1 is capacitor from 0.1uF to 2.2uF depends on the kind of Vdd source and sound loudness.
   E.g. If COUT is used, C1 can be 0.1uF. However, if PWM direct drive speaker is used, C1 should be at least 2.2uF
1 Rb is base resistor from 120 Ohm to 390 Ohm depends on Vdd value and transistor gain.
2 Tr is an NPN transistor with beta larger than 150, e.g. 8050D.
3 Rosc depending on sampling rate (see oscillator frequency table)

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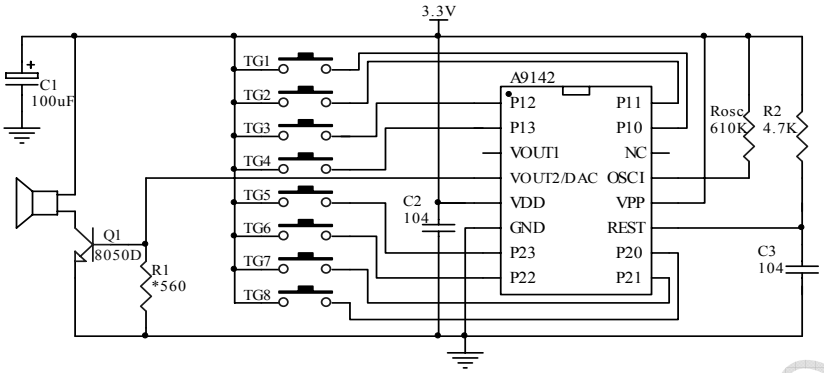
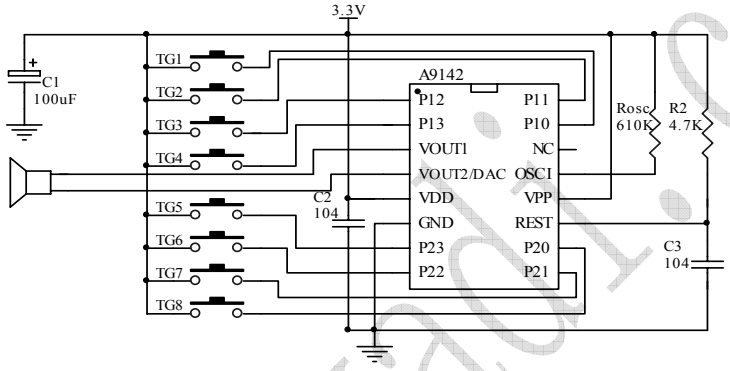
APPLICATION CIRCUIT

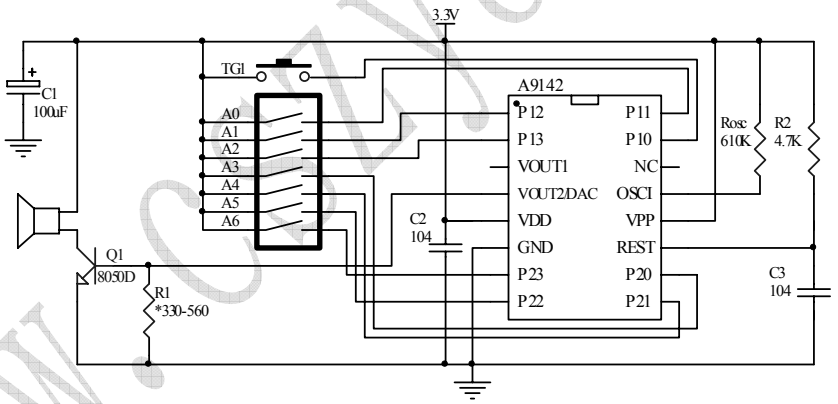
A9142 DIP16 ALONE 8KEY DAC OUTPUT TEST CIRCUIT



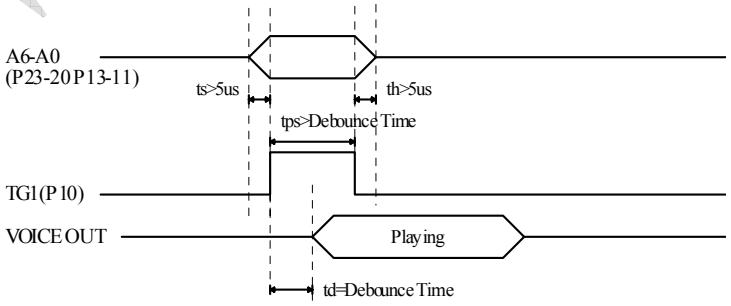
A9142 DIP16 ALONE 8KEY PWM DRIVER TEST CIRCUIT



A9142 DIP16 CPU Parallel Mode TEST CIRCUIT



TIMING DIAGRAM



*CPU parallel address mode trigger up to 128 voice groups any combination of trigger options.
*Debounce time is inversely proportional to Sampling Rate, e.g. 24ms at 8KHz sampling rate.

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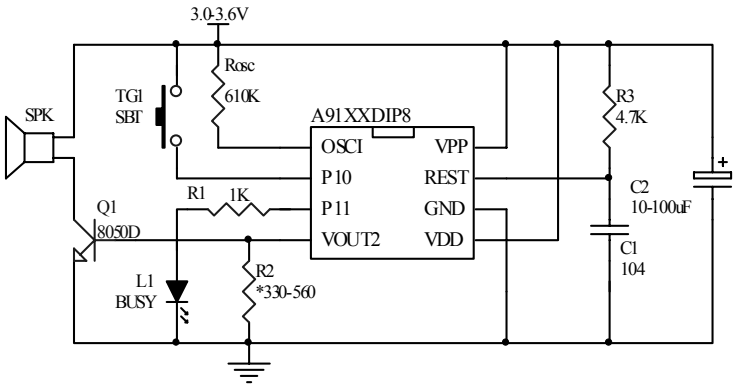
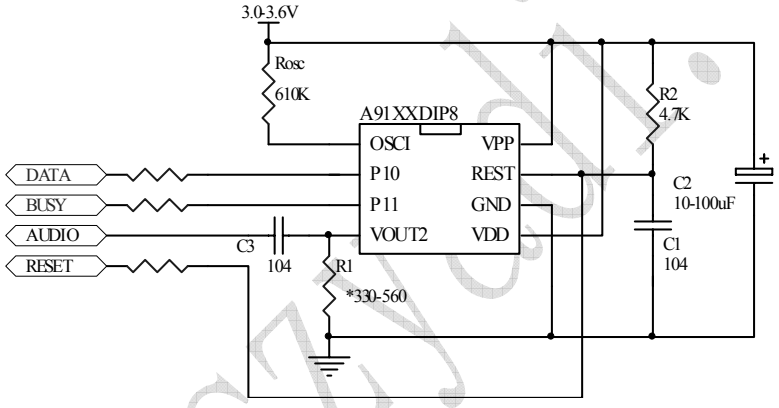
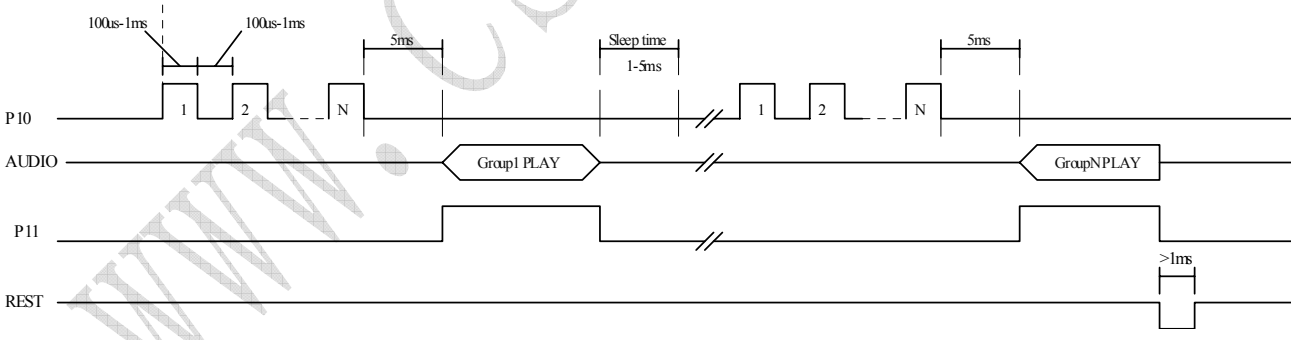
A9142 DIP8 ALONE 1KEY SBT TEST CIRCUIT



A9142 DIP8 MCU 1LINE PULSE MODE TEST CIRCUIT



TIMING DIAGRAM



Note: P10 must goes back to LOW otherwise the chip will not enter stand-by state after playback.

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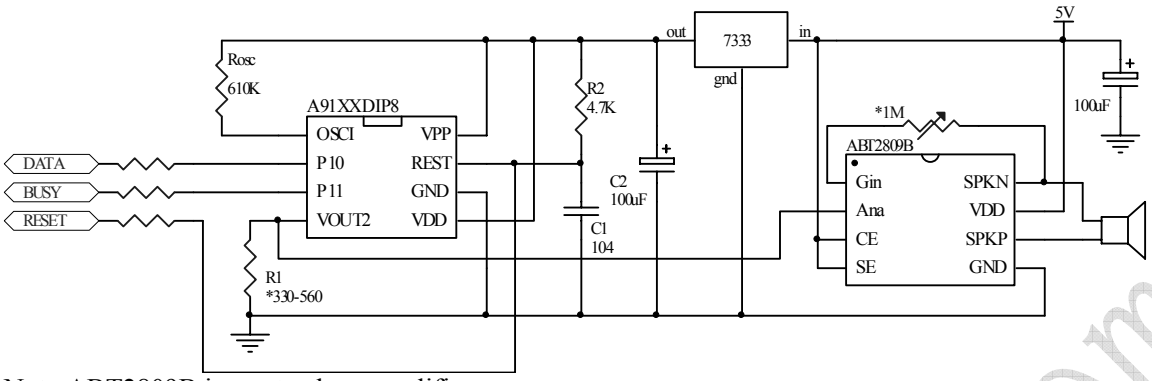
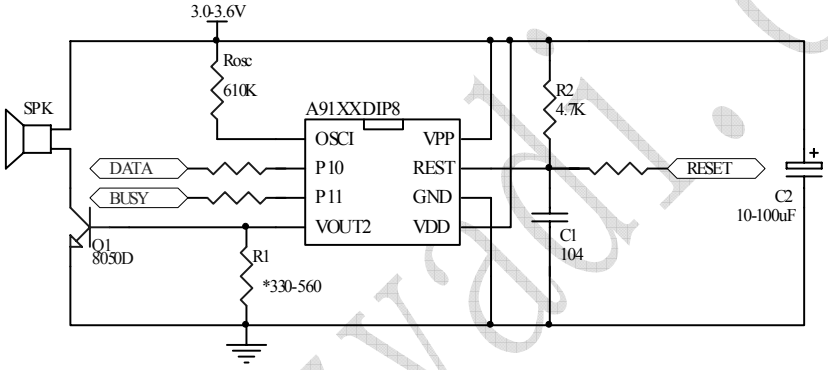
A9142 DIP8 MCU 1LINE MODE AND ABT2809B TEST CIRCUIT

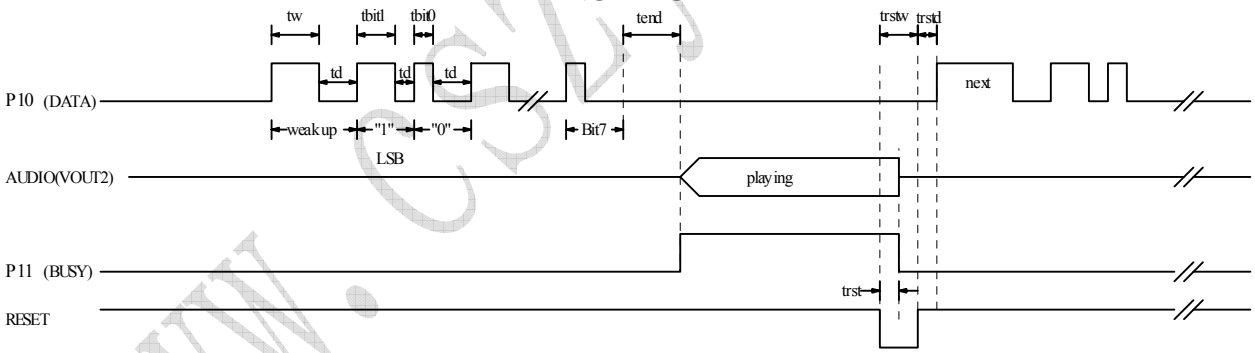


Note:ABT2809B is a auto sleep amplifier.

A9142 DIP8 MCU 1LINE DATA MODE TEST CIRCUIT



TIMING DIAGRAM



AC Characteristics

Symbol	Description	Min.	Typ.	Max.
tw	Weak up pulse width	1.2ms	--	--
tbit0	Pulse width of logical data '0'	300us	400us	500us
tbit1	Pulse width of logical data '1'	700us	800us	900us
td	Delay time to next data bit input	100us	--	--
tend	End of last data bit time	5ms	--	--
trstw	Pulse width of reset signal	1ms	--	--
trst	Time to voice out stop	--	1ms	--
trstd	Delay time to next data bit after reset	1ms	--	--

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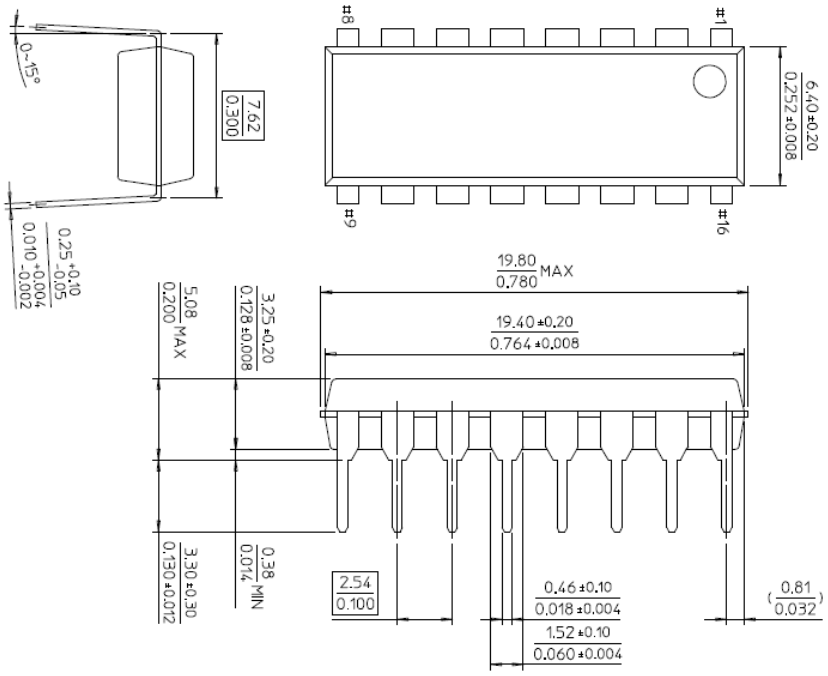
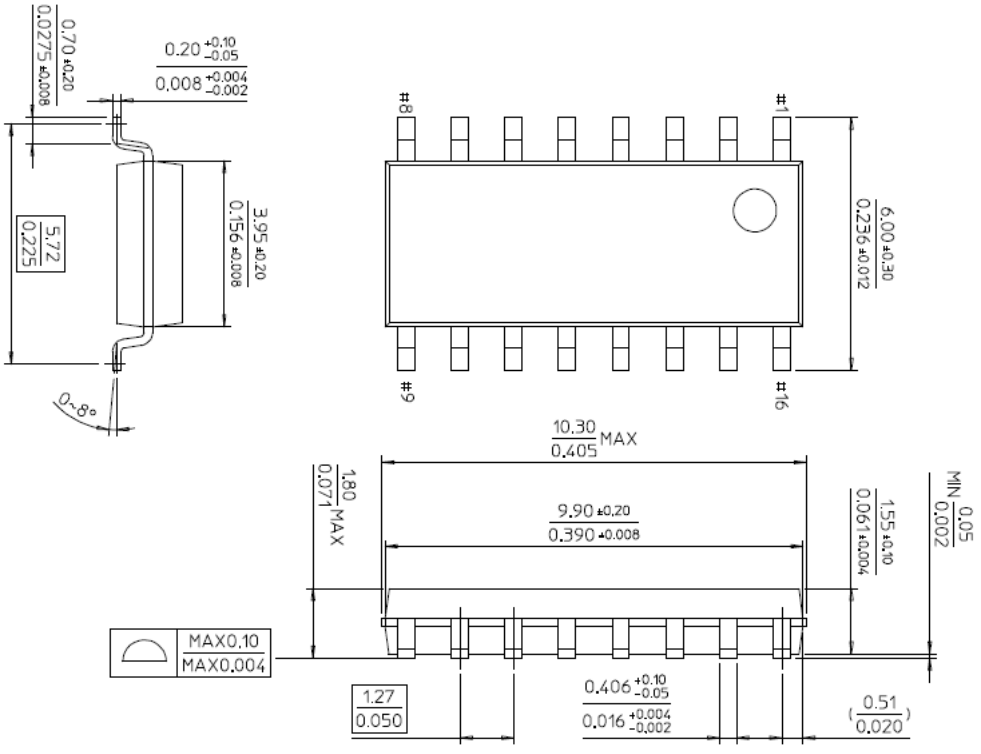
PACKAGES LIST

16-Pin 300mil P-DIP Package



16-Pin 150mil SOP Package



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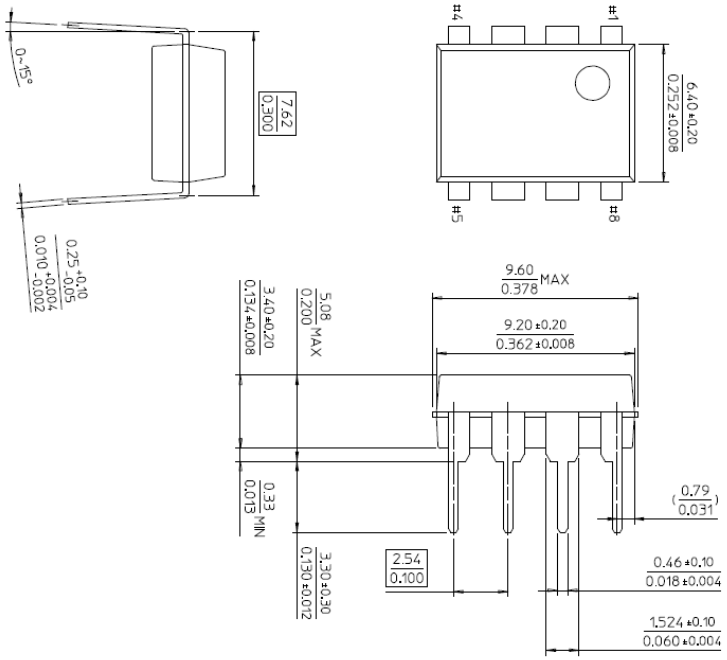
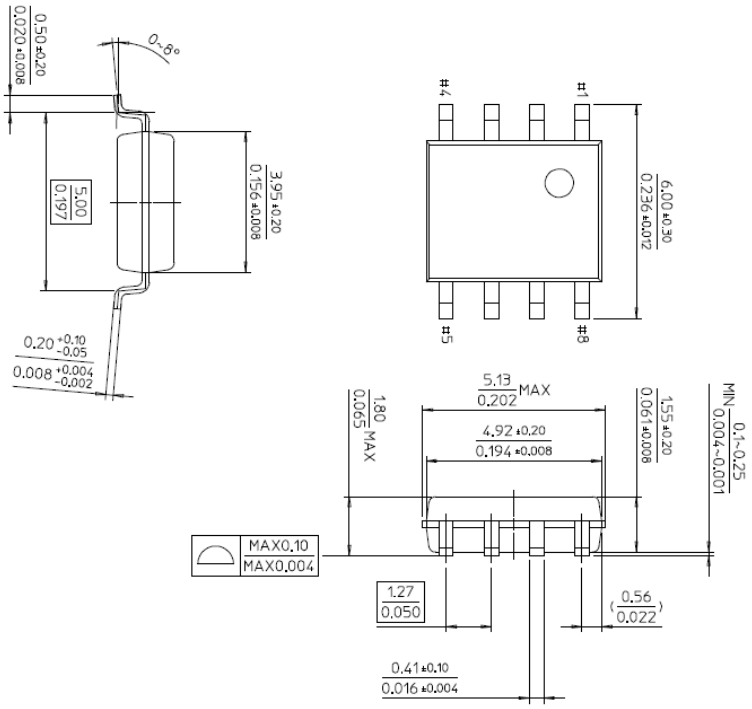
8-Pin 300mil P-DIP Package



8-Pin 150mil SOP Package



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